DATA SHEET

NE56605-42
System reset with built-in watchdog timer

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File under Integrated Circuits, Standard Analog

Philips
Semiconductors

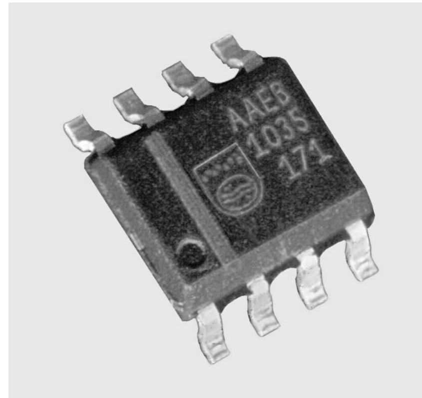
PHILIPS

System reset with built-in watchdog timer NE56605-42

GENERAL DESCRIPTION

The NE56605-42 is designed to generate a reset signal, at a threshold voltage of 4.2 V, for a variety of microprocessor and logic systems. Accurate reset signals are generated during momentary power interruptions, or whenever power supply voltages sag to intolerable levels. The NE56605-42 has a built-in Watchdog Timer to monitor the microprocessor and ensure it is operating properly. Any abnormal system operations due to microprocessor malfunctions are terminated by the watchdog's generating a system reset. The NE56605-42 has a watchdog monitoring time of 10 ms (typical).

The NE56605-42 is offered in the SO8 surface mount package.



FEATURES

- Both positive and negative logic reset output signals are available
- Accurate threshold detection
- Internal power-on reset delay
- Internal watchdog timer programmable with external capacitor
- Watchdog monitoring time of 10 ms
- Reset assertion with V_{CC} down to 0.8 V_{DC} (typical)
- Few external components required.

APPLICATIONS

- Microcomputer systems
- Logic systems.

SIMPLIFIED SYSTEM DIAGRAM

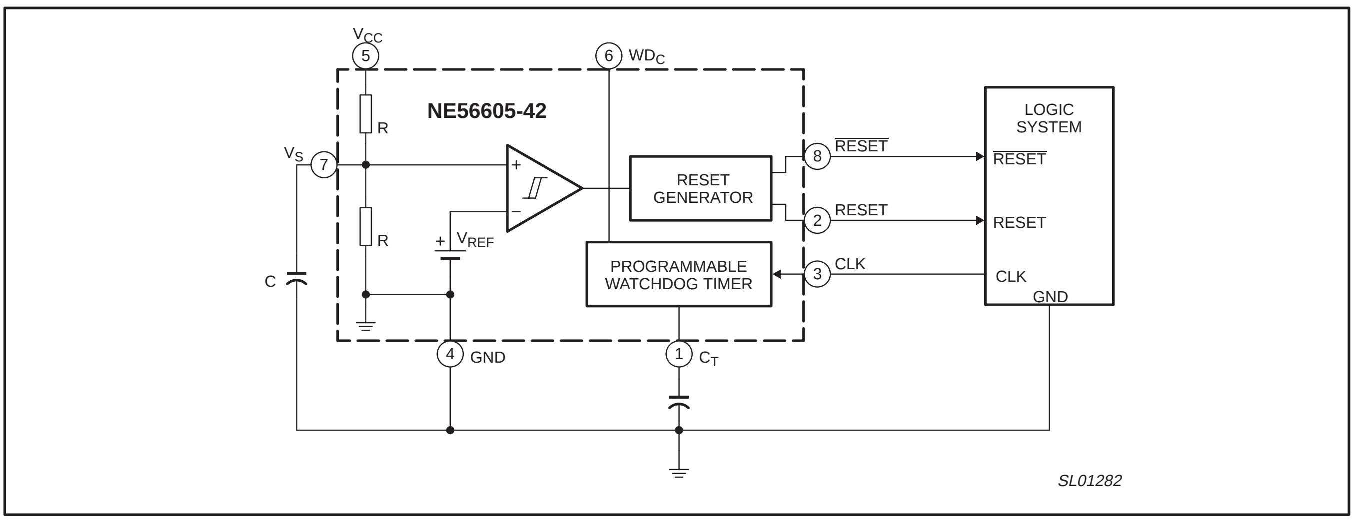


Figure 1. Simplified system diagram.

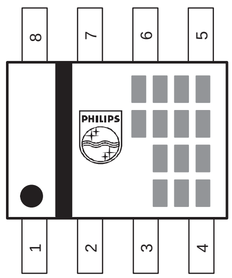
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE
	NAME	DESCRIPTION	
NE56605-42D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	–20 to +70 °C

System reset with built-in watchdog timer NE56605-42

Part number marking

The package is marked with a four letter code in the first line to the right of the logo. The first three letters designate the product. The fourth letter, represented by ‘x’, is a date tracking code. The remaining two or three lines of characters are internal manufacturing codes.



Part number	Marking
NE56605-42	A A E x

PIN CONFIGURATION

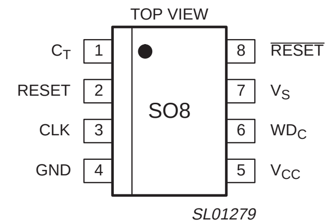


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	C_T	t_{WDM}, t_{WDR}, t_{PR} adjustment pin. t_{WDM}, t_{WDR}, t_{PR} times are dependent on the value of external C_T capacitor used. See Figure 18 (Timing Diagram) for definition of t_{WDM}, t_{WDR}, t_{PR} times.
2	RESET	Reset HIGH output pin.
3	CLK	Clock input pin from logic system for watchdog timer.
4	GND	Circuit ground.
5	V_{CC}	Power supply pin for circuit.
6	WD_C	Watchdog timer control pin. The watchdog timer is enabled when this pin is unconnected, and disabled when this pin is connected to ground.
7	V_S	Detection threshold adjustment pin. The detection threshold can be increased by connecting this pin to V_{CC} with a pull-up resistor. The detection threshold can be decreased by connecting this pin to ground with a pull-down resistor.
8	$\overline{\text{RESET}}$	Reset LOW output pin.

MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	Power supply voltage	–0.3	10	V
V_S	V_S pin voltage	–0.3	10	V
V_{CLK}	CLK pin voltage	–0.3	10	V
V_{OH}	RESET and $\overline{\text{RESET}}$ pin voltage	–0.3	10	V
T_{oper}	Operating temperature	–20	70	°C
T_{stg}	Storage temperature	–40	125	°C
P	Power dissipation	–	250	mW

DC ELECTRICAL CHARACTERISTICS

Characteristics measured with V_{CC} = 5.0 V, and T_{amb} = 25 °C, unless otherwise specified.
See Figure 23 (Test circuit 1) for test configuration used for DC parameters.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CC}	Supply current during watchdog timer operation		–	0.7	1.0	mA
V_{SL}	Reset detection threshold	V_S = open; V_{CC} = falling	4.05	4.20	4.35	V
V_{SH}	Reset detection threshold	V_S = open; V_{CC} = rising	4.15	4.30	4.45	V
$\Delta V_S/\Delta T_{amb}$	Temperature coefficient of reset threshold	–20 °C ≤ T_{amb} ≤ 70 °C	–	±0.01	–	%/°C
V_{hys}	Reset threshold hysteresis	V_{HYS} = V_{SH} (rising V_{CC}) – V_{SL} (falling V_{CC})	50	100	150	mV
V_{TH}	CLK input threshold		0.8	1.2	2.0	V
I_{IH}	CLK input current, HIGH-level	V_{CLK} = 5.0 V	–	0	1.0	µA
I_{IL}	CLK input current, LOW-level	V_{CLK} = 0 V	–20	–10	–3.0	µA
V_{OH1}	Output voltage, HIGH-level	$I_{\overline{RESET}}$ = –5.0 µA; V_S = open	4.5	4.8	–	V
V_{OH2}		I_{RESET} current = –5.0 mA; V_S = 0 V	4.5	4.8	–	V
V_{OL1}	Output voltage, LOW-level	$I_{\overline{RESET}}$ = 3.0 mA; V_S = 0 V	–	0.2	0.4	V
V_{OL2}		$I_{\overline{RESET}}$ = 10 mA; V_S = 0 V	–	0.3	0.5	V
V_{OL3}		I_{RESET} = 0.5 mA; V_S = open	–	0.2	0.4	V
V_{OL4}		I_{RESET} = 1.0 mA; V_S = open	–	0.3	0.5	V
I_{OL1}	Output sink current	$V_{\overline{RESET}}$ = 1.0 V; V_S = 0 V	10	16	–	mA
I_{OL2}		V_{RESET} = 1.0 V; V_S = open	1.0	2.0	–	mA
I_{CT1}	C_T charge current	V_{CT} = 1.0 V; WD_C = open during watchdog operation	–8	–12	–24	µA
I_{CT2}		V_{CT} = 1.0 V; during power-on reset operation	–0.8	–1.2	–2.4	µA
V_{CCL1}	Supply voltage to assert reset operation	$V_{\overline{RESET}}$ = 0.4 V; $\overline{RESET}$ current = 0.2 mA	–	0.8	1.0	V
V_{CCL2}		V_{RESET} = V_{CC} – 0.1 V; 1 MΩ resistor (pin 2 to GND)	–	0.8	1.0	V

AC ELECTRICAL CHARACTERISTICS

Characteristics measured with V_{CC} = 5.0 V, and T_{amb} = 25 °C, unless otherwise specified.
See Figure 24 (Test circuit 2) for test configuration used for AC parameters.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{P1}	Minimum power supply pulse width for detection	4.0 V ≤ negative-going V_{CC} pulse ≤ 5.0 V	8.0	–	–	µs
t_{CLKW}	Clock input pulse width		3.0	–	–	µs
t_{CLK}	Clock input cycle		20	–	–	µs
t_{WDM}	Watchdog monitoring time (Notes 1, 6)	C_T = 0.1 µF; R_{CT} = open	5.0	10	15	ms
t_{WDR}	Watchdog reset time (Notes 2, 6)	C_T = 0.1 µF	1.0	2.0	3.0	ms
t_{PR}	Power-on reset delay time (Notes 3, 6)	V_{CC} = rising from 0 V; C_T = 0.1 µF	50	100	150	ms
t_{PD1}	RESET, $\overline{RESET}$ propagation delay time (Note 4)	$\overline{RESET}$: R_{L1} = 2.2 kΩ; C_{L1} = 100 pF	–	2.0	10	µs
t_{PD2}		RESET: R_{L2} = 10 kΩ; C_{L2} = 20 pF	–	3.0	10	µs
t_{R1}	RESET, $\overline{RESET}$ rise time (Note 5)	$\overline{RESET}$: R_{L1} = 2.2 kΩ; C_{L1} = 100 pF	–	1.0	1.5	µs
t_{R2}		RESET: R_{L2} = 10 kΩ; C_{L2} = 20 pF	–	1.0	1.5	µs
t_{F1}	RESET, $\overline{RESET}$ fall time (Note 5)	$\overline{RESET}$: R_{L1} = 2.2 kΩ; C_{L1} = 100 pF	–	0.1	0.5	µs
t_{F2}		RESET: R_{L2} = 10 kΩ; C_{L2} = 20 pF	–	0.5	1.0	µs

NOTES:

1. 'Watchdog monitoring time' is the duration from the last pulse (negative-going edge) of the timer clear clock pulse until reset output pulse occurs (see Figure 18). A reset signal is output if a clock pulse is not input during this time.
2. 'Watchdog reset time' is the reset pulse width (see Figure 18).
3. 'Power-on reset delay time' is the duration measured from the time V_{CC} exceeds the upper detection threshold (V_{SH}) and power-on reset release is experienced ($\overline{RESET}$ output HIGH; RESET output LOW).
4. 'RESET, $\overline{RESET}$ propagation delay time' is the duration from when the supply voltage sags below the lower detection threshold (V_{SL}) and reset occurs ($\overline{RESET}$ output LOW, RESET output HIGH).
5. RESET, $\overline{RESET}$ rise and fall times are measured at 10% and 90% output levels.
6. Watchdog monitoring time (t_{WDM}), watchdog reset time (t_{WDR}), and power-on reset delay time (t_{PR}) during power-on can be modified by varying the C_T capacitance. The times can be approximated by applying the following formula. The recommended range for C_T is 0.001 µF to 10 µF.

Formula 1. Calculation for approximate t_{PR}, t_{WDM}, and t_{WDR} values:

t_{PR} (ms) ≈ 1000 × C_T (µF)
t_{WDM} (ms) ≈ 100 × C_T (µF)
t_{WDR} (ms) ≈ 20 × C_T (µF)

Example: When C_T = 0.1 µF and WD_C = open:

t_{PR} ≈ 100 ms
t_{WDM} ≈ 10 ms
t_{WDR} ≈ 2.0 ms

TYPICAL PERFORMANCE CURVES

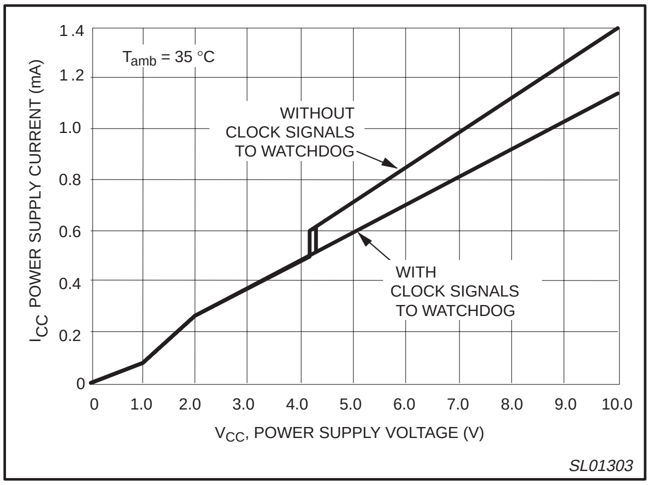


Figure 3. Power supply current versus voltage.

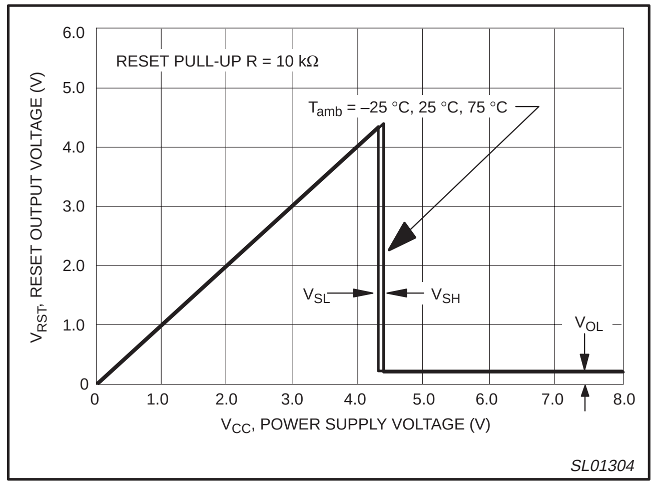


Figure 4. RESET output voltage versus supply voltage.

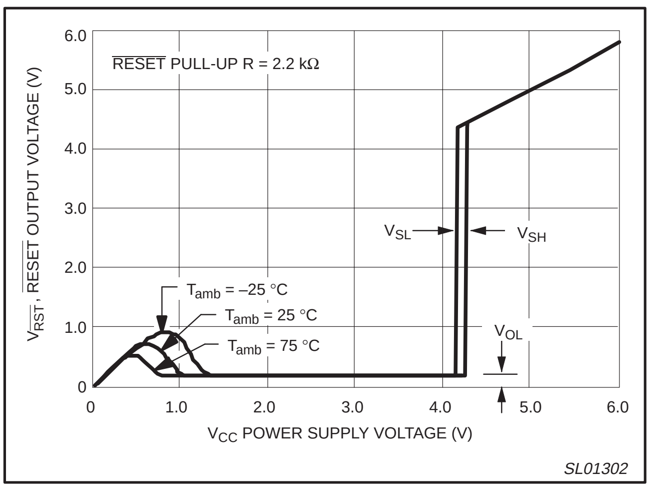


Figure 5. $\overline{\text{RESET}}$ output voltage versus supply voltage.

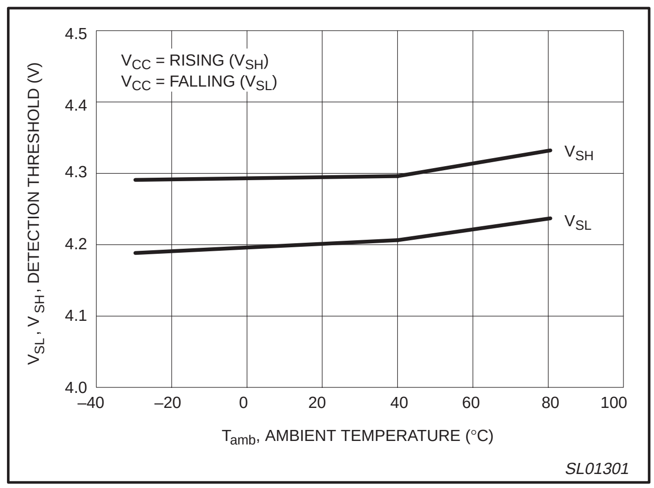


Figure 6. Detection threshold versus temperature.

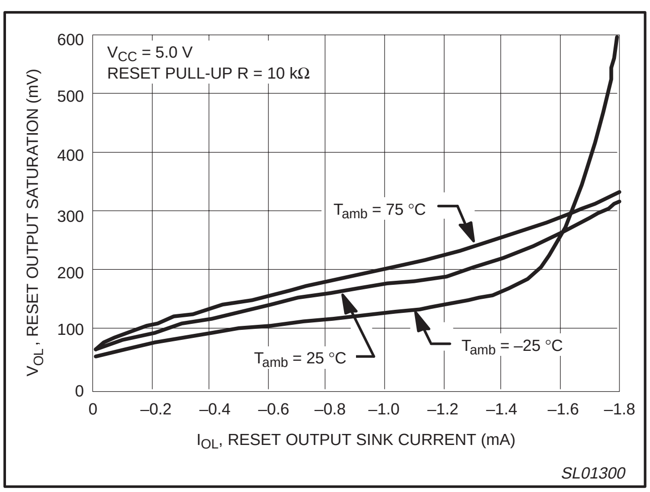


Figure 7. RESET saturation versus sink current.

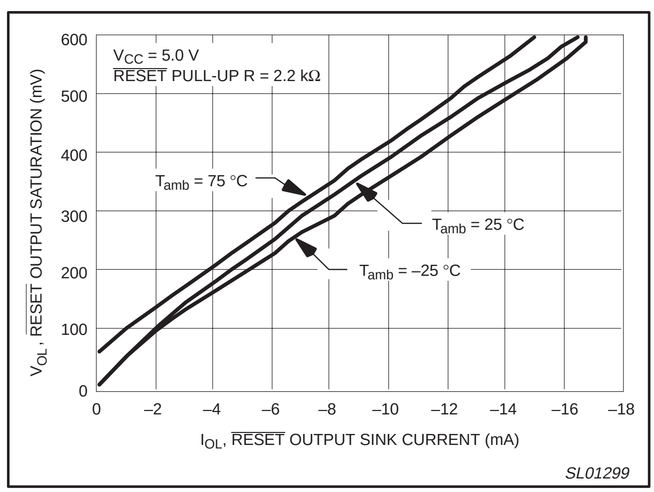


Figure 8. $\overline{\text{RESET}}$ saturation versus sink current.

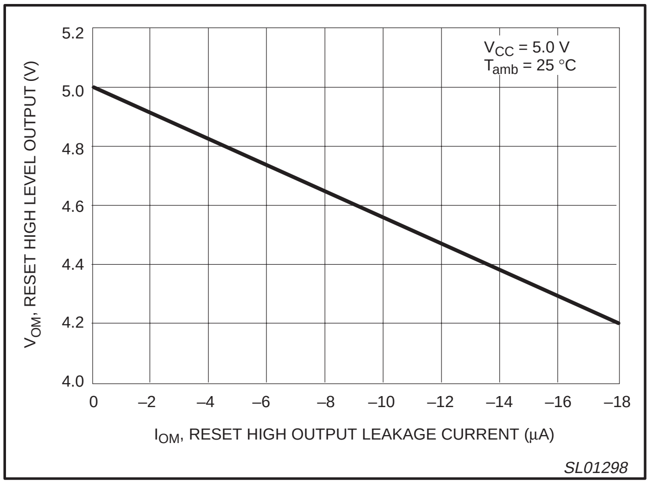


Figure 9. RESET HIGH-level voltage versus current.

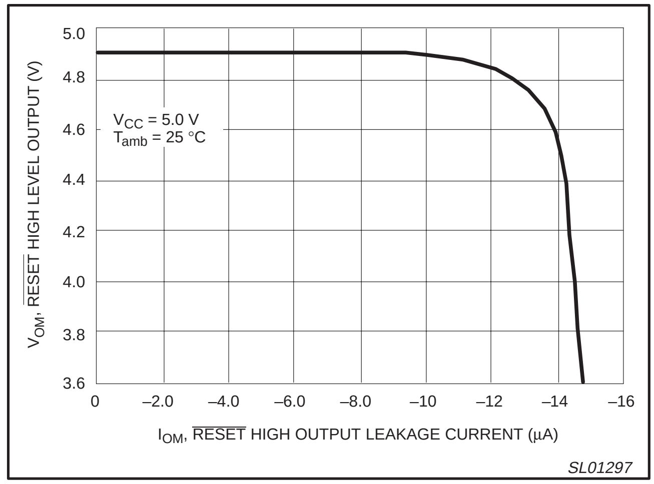


Figure 10. RESET HIGH-level voltage versus current.

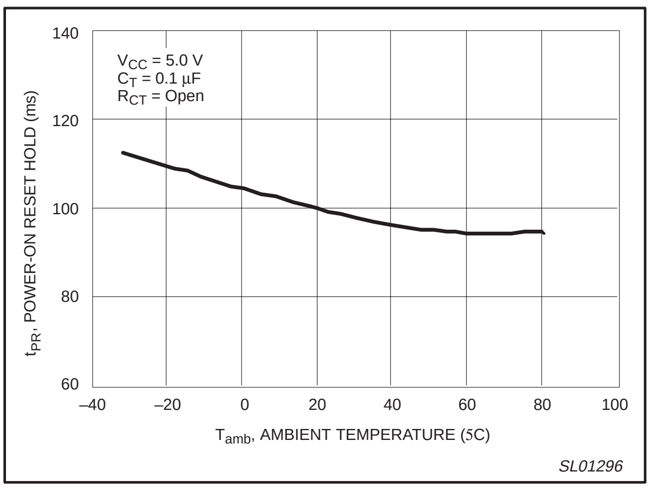


Figure 11. Power–on reset hold time versus temperature.

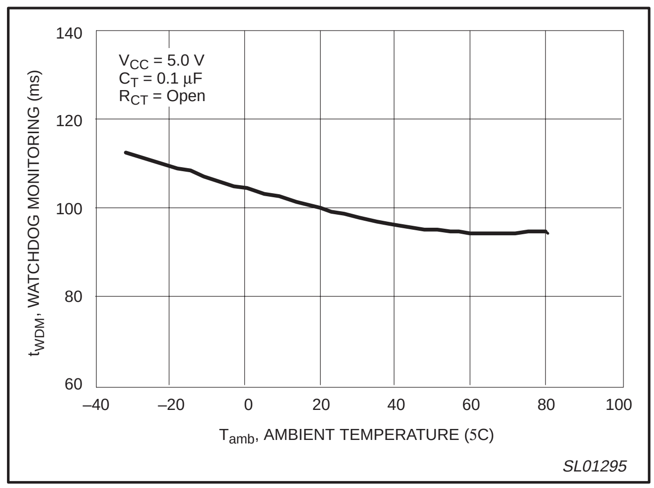


Figure 12. Watchdog monitoring time versus temperature.

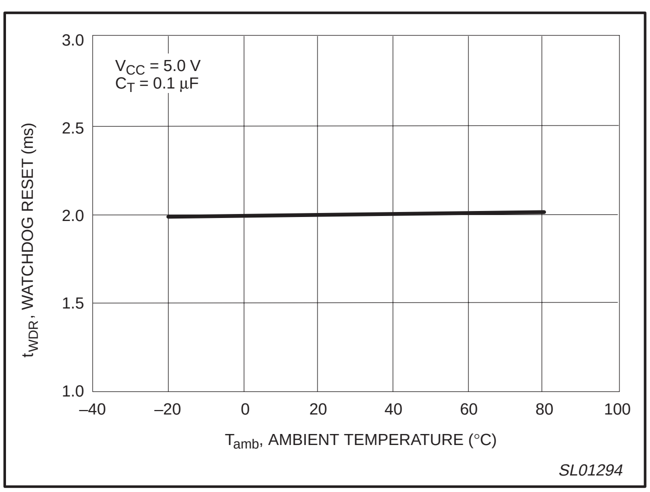


Figure 13. Watchdog reset time versus temperature.

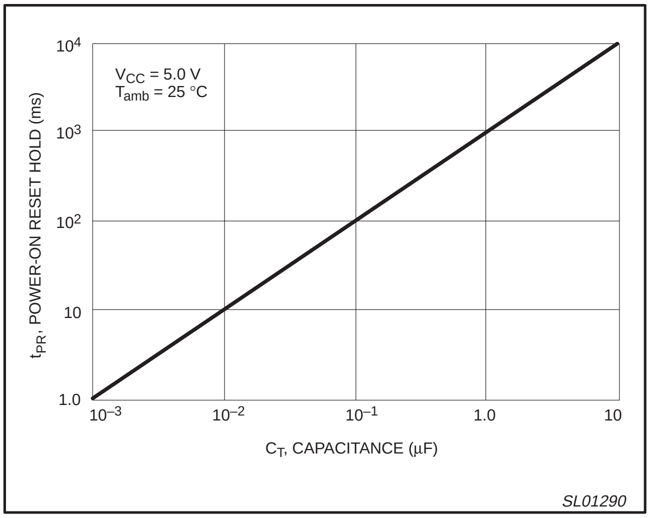


Figure 14. Power-on reset hold time versus C_T.

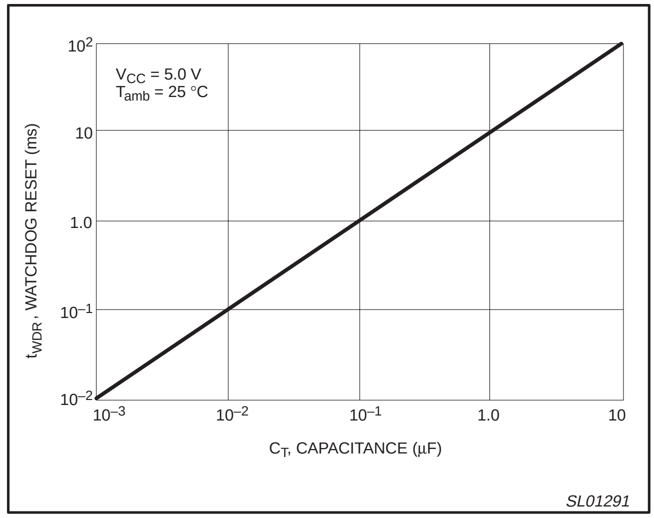


Figure 15. Watchdog reset time versus C_T.

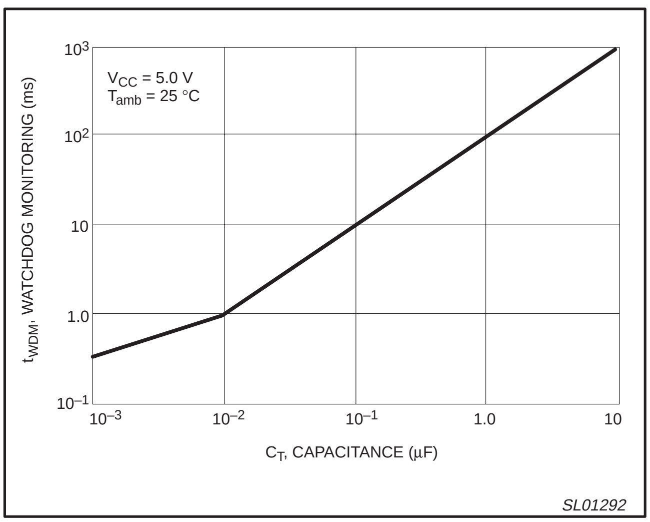


Figure 16. Watchdog reset time versus C_T.

TECHNICAL DESCRIPTION

General discussion

The NE56605-42 combines a watchdog timer and an undervoltage reset function in a single SO8 surface mount package. This provides a space-saving solution for maintaining proper operation of typical 5.0 volt microprocessor-based logic systems. Either function, or both, can force the microprocessor into a reset.

While the watchdog monitors the microprocessor operation, the undervoltage reset monitors the supply voltage to the microprocessor. If the microprocessor clock signal ceases or becomes erratic, the NE56605-42 outputs a reset signal to the microprocessor. If the microprocessor supply voltage sags to 4.2 volts or less, the NE56605-42 outputs a reset signal for the duration of the supply voltage deficiency. The undervoltage reset signal allows the microprocessor to shut down in an orderly manner to avoid system corruption. In addition to a single reset output, the NE56605-42 has complementary $\overline{\text{RESET}}$ and RESET outputs for system use. The undervoltage detection threshold incorporates hysteresis to prevent generating erratic resets.

The watchdog timer requires a pulse input. Normally this signal comes from the system microprocessor's clock. For operation, an external capacitor (C_T) must be connected from Pin 1 to ground. Normally a 0.1 µF capacitor is used for C_T. The C_T capacitor and a fixed internal resistance establish the required minimum frequency of watchdog input signal for the device to **not** output a reset signal. In the absence of a watchdog input pulse, the C_T capacitor charges to the 0.2 volt threshold of the internal comparator, causing a reset signal to be output. If microprocessor clock signals are received within the required interval, no watchdog reset signal will be output. Grounding the watchdog control pin (WD_C, Pin 6) disables the watchdog function. Removing the ground from Pin 6, allowing it to float, enables the watchdog function. Enabling or disabling the watchdog function has no effect on the undervoltage detection function.

Although the temperature coefficient of detection threshold is specified over a temperature of –20 °C to +70 °C, the device will support operation in excess of this temperature range. See the supporting curves for performance over the full temperature range of –30 °C to +85 °C. Some degradation in performance will be experienced at the temperature extremes and the system designer should take this into account.

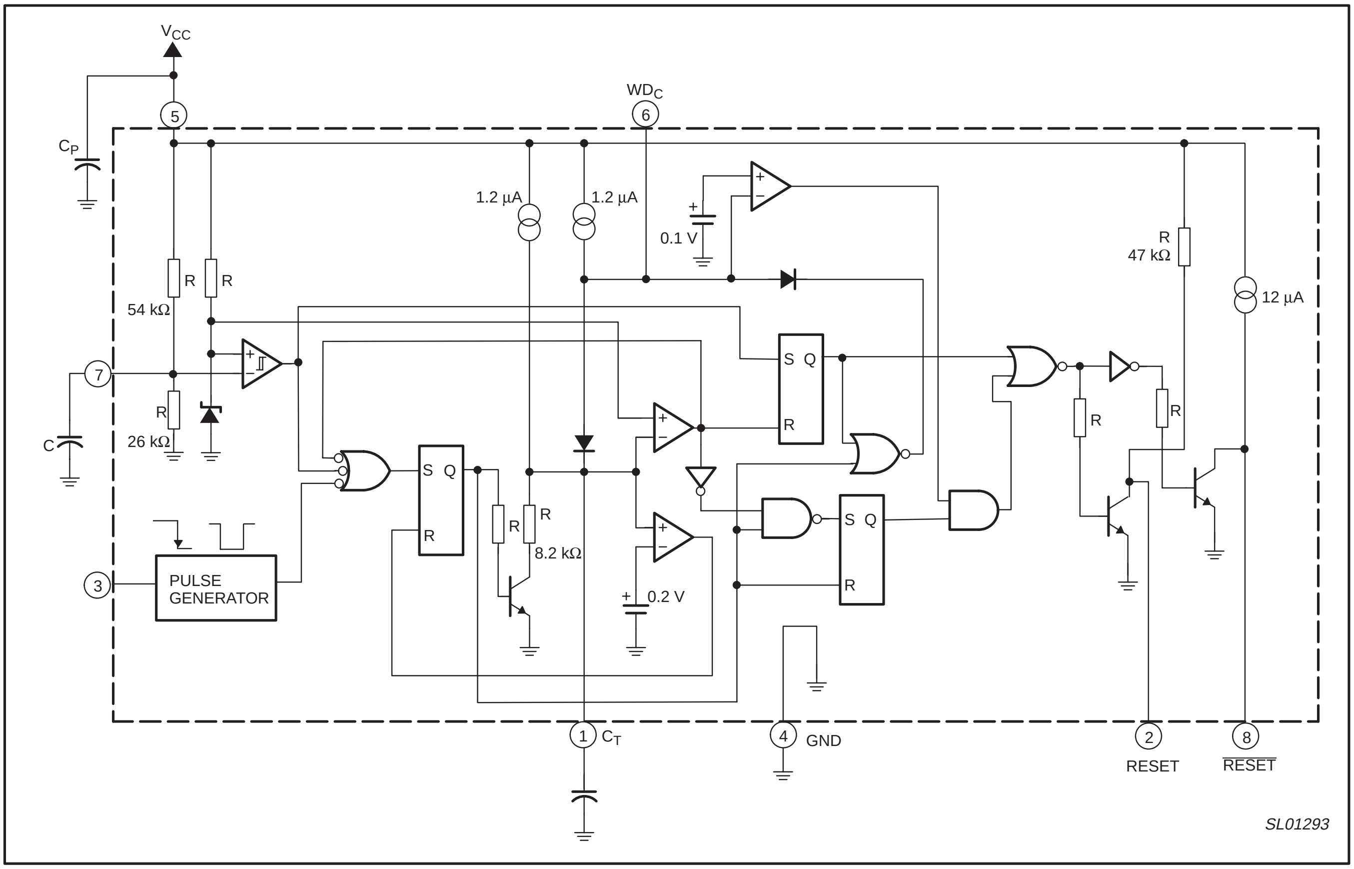


Figure 17. Functional diagram.

Timing diagram

The timing diagram shown in Figure 18 depicts the operation of the device. Letters indicate events on the TIME axis.

A: At start-up ‘A’, the V_{CC} and RESET voltages begin to rise. Also the $\overline{\text{RESET}}$ voltage initially rises, but then abruptly returns to a LOW state. This is due to V_{CC} reaching the level (approximately 0.8 V) that activates the internal bias circuitry, asserting $\overline{\text{RESET}}$.

B: Just before ‘B’, the C_T voltage starts to ramp up. This is caused by, and coincident to, V_{CC} reaching the threshold level of V_{SH}. At this level the device is in full operation. The RESET output continues to rise as V_{CC} rises above V_{SH}. This is normal.

C: At ‘C’, V_{CC} is above the undervoltage detect threshold, and C_T has ramped up to its upper detect level. At this point, the device removes the hold on the resets. $\overline{\text{RESET}}$ goes HIGH while RESET goes LOW. Also, an internal ramp discharge transistor activates, discharging C_T.

In a microprocessor-based system these events remove the reset from the microprocessor, allowing it to function normally. The system must send clock signals to the Watchdog Timer often enough to prevent C_T from ramping up to the C_T threshold, to prevent reset signals from being generated. Each clock signal discharges C_T.

C–D: Midway between ‘C’ and ‘D’, the CLK signals cease allowing the C_T voltage to ramp up to its upper threshold at ‘D’. At this time, reset signals are generated ($\overline{\text{RESET}}$ goes LOW; RESET goes HIGH). The device attempts to come out of reset as the C_T voltage is discharged and finally does come out of reset when CLK signals are re-established after two attempts of C_T.

E–F: Immediately before ‘E’, falling V_{CC} causes the $\overline{\text{RESET}}$ signal to sag. CLK signals are still being received, C_T is within normal operating range, and reset signals are not output. V_{CC} continues to sag until the V_{SL} undervoltage threshold is reached. At that time, reset signals are generated ($\overline{\text{RESET}}$ goes LOW; RESET goes HIGH).

At ‘E’, V_{CC} starts to rise, and the Reset voltage rises with V_{CC}. However, C_T voltage does not start to ramp up until ‘F’ when V_{CC} reaches the V_{SH} upper threshold.

G: The reset outputs are released at ‘G’ when C_T reaches the upper threshold level again. After ‘G’, normal CLK signals are received, but at a lower frequency than those following event ‘C’. The frequency is above the minimum frequency required to keep the device from outputting reset signals.

G–H: At ‘H’, V_{CC} is normal, CLK signals are being received, and no reset signals are output. At event ‘H’, the V_{CC} starts falling, causing $\overline{\text{RESET}}$ to also fall.

J: At event ‘J’, V_{CC} sags to the point where the V_{SL} undervoltage threshold point is reached, and at that level reset signals are output ($\overline{\text{RESET}}$ to a LOW state, and RESET to a HIGH state). As the V_{CC} voltage falls lower, the Reset voltage falls lower.

K: At event ‘K’, the V_{CC} voltage has deteriorated to a level where normal internal circuit bias is no longer able to maintain a $\overline{\text{RESET}}$, and as a result may exhibit a slight rise to something less than 0.8 V. As V_{CC} decays even further, $\overline{\text{RESET}}$ also decreases to zero.

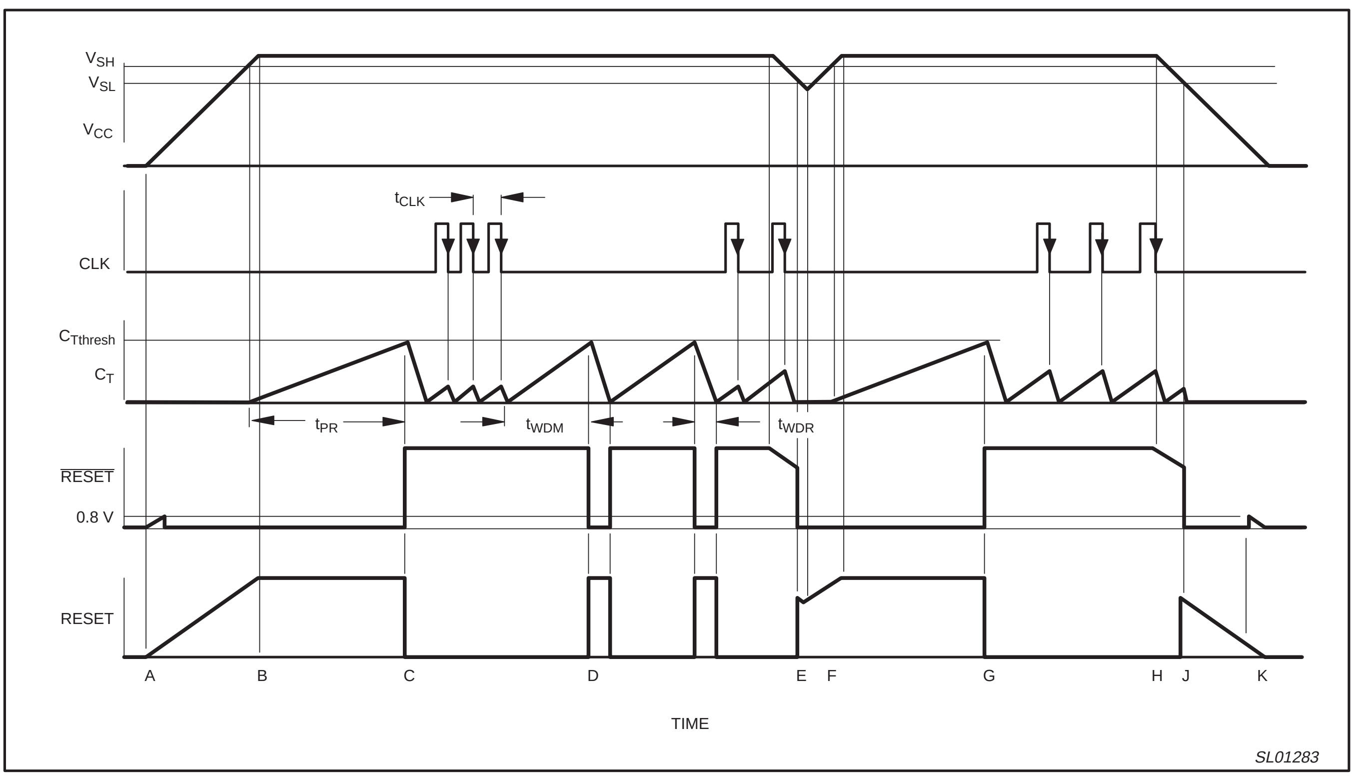


Figure 18. Timing diagram.

Application information

The detection threshold voltage can be adjusted by externally influencing the internal divider reference voltage. Figures 19 and 21 show a method to lower and raise the threshold voltage. Figures 20 and 22 show the influence of the pull-down and pull-up resistors on the threshold voltage. The use of a capacitor (1000 pF or larger) from Pin 7 to ground is recommended to filter out noise from being imposed on the threshold voltages.

The Reset Detection Threshold can be decreased by connecting an external resistor R_1 from Pin 7 to V_{CC}, as shown in Figure 19. See Figure 20 to determine the approximate value of R_1 to use.

The Reset Detection Threshold can be increased by connecting an external resistor R_2 from Pin 7 to ground, as shown in Figure 21. See Figure 22 to determine the approximate value of R_2 to use.

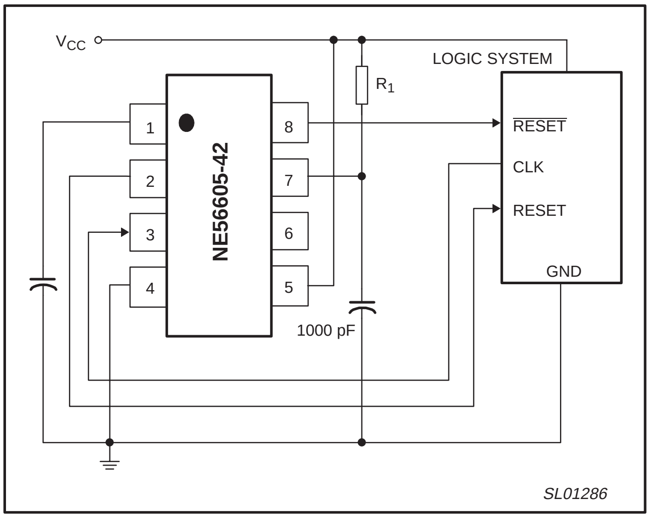


Figure 19. Circuit to lower detection threshold.

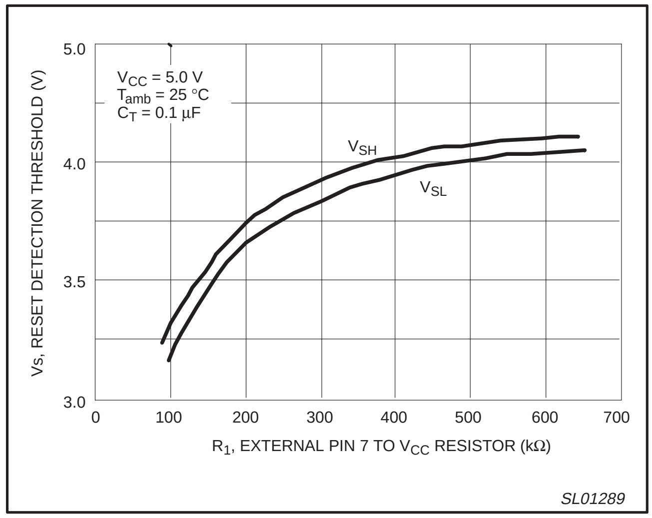


Figure 20. Reset detection threshold versus external R_1.

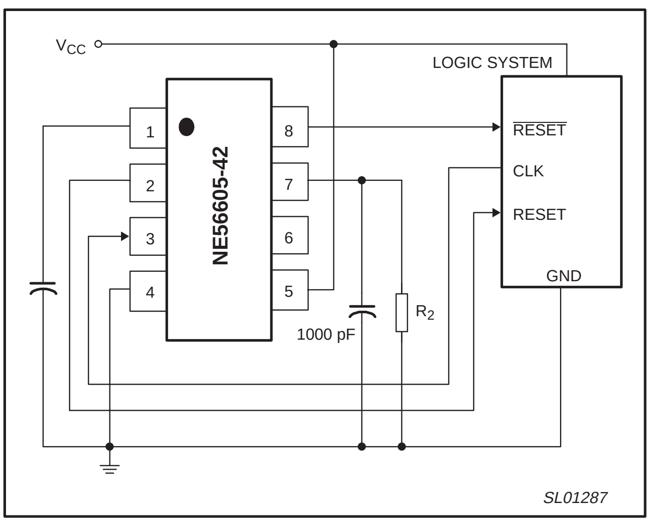


Figure 21. Circuit to raise detection threshold.

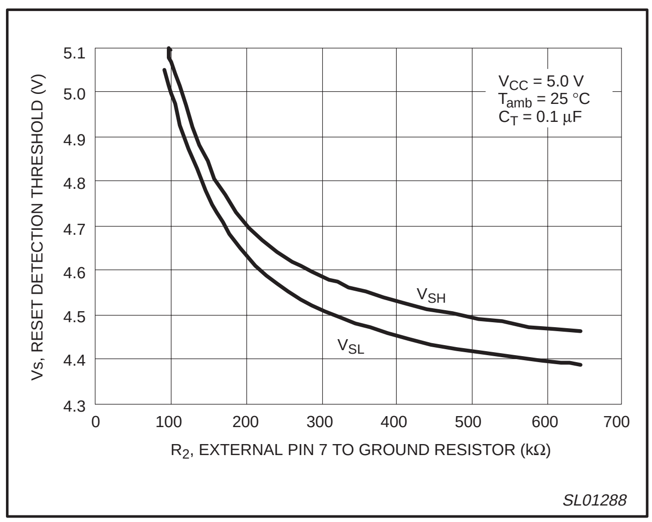


Figure 22. Reset detection threshold versus external R_2.

Parametric testing

DC and AC Characteristics can be tested using the circuits shown in Figures 23 and 24. Associated switch and power supply settings are shown in Table 1 and Table 2, respectively.

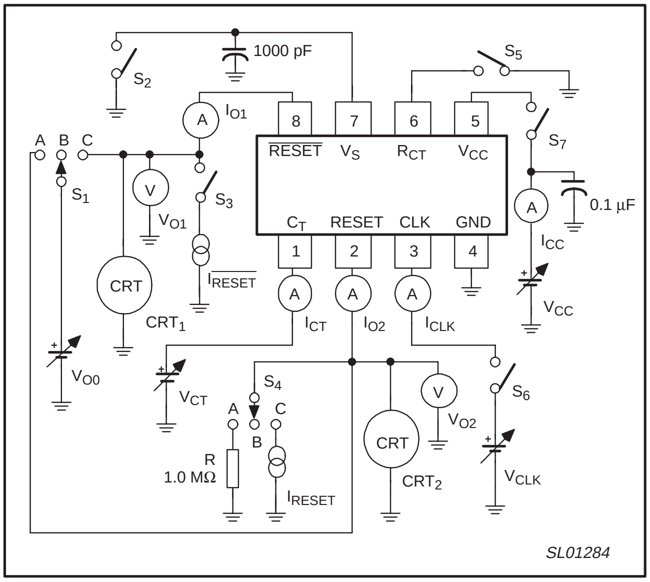


Figure 23. Test Circuit 1 (DC parameters).

Table 1. DC characteristics Test Circuit 1 switch and power supply settings

Parameter	Symbol	S_1	S_2	S_3	S_4	S_5	S_6	S_7	V_{CC}	V_{CLK}	V_{CT}	$I_{\overline{RESET}}$	I_{RESET}	Read
Power supply current	I_{CC}	B	OFF	OFF	B	OFF	ON	ON	5.0 V	5.0 V	0 V	–	–	I_{CC}
Reset threshold (LOW) (Note 1)	V_{SL}	B	OFF	OFF	B	ON	ON	ON	5.0 to 4.0 V	3.0 V	3.0 V	–	–	V_{O1}, CRT_1
Reset threshold (HIGH) (Note 2)	V_{SH}	B	OFF	OFF	B	ON	ON	ON	4.0 to 5.0 V	3.0 V	3.0 V	–	–	V_{O1}, CRT_1
Clock input threshold (Note 3)	V_{TH}	B	OFF	OFF	B	OFF	ON	ON	5.0 V	0 to 3.0 V	1.0V	–	–	I_{CLK}
Clock input current (HIGH)	I_{TH}	B	OFF	OFF	B	OFF	ON	ON	5.0 V	5.0 V	0 V	–	–	I_{CLK}
Clock input current (LOW)	I_{TL}	B	OFF	OFF	B	OFF	ON	ON	5.0 V	0 V	0 V	–	–	I_{CLK}
Reset output voltage (HIGH)	V_{OH1}	B	OFF	ON	B	ON	ON	ON	5.0 V	5.0 V	3.0 V	–5.0 µA	–	V_{O1}
	V_{OH2}	B	ON	OFF	C	ON	ON	ON	5.0 V	5.0 V	3.0 V	–	–5.0 µA	V_{O2}
Reset output voltage (LOW)	V_{OL1}	B	ON	ON	B	ON	ON	ON	5.0 V	5.0 V	3.0 V	3.0 mA	–	V_{O1}
	V_{OL2}	B	ON	ON	B	ON	ON	ON	5.0 V	5.0 V	3.0 V	10 mA	–	V_{O1}
	V_{OL3}	B	OFF	OFF	C	ON	ON	ON	5.0 V	5.0 V	3.0 V	–	0.5 mA	V_{O2}
	V_{OL4}	B	OFF	OFF	C	ON	ON	ON	5.0 V	5.0 V	3.0 V	–	1.0 mA	V_{O2}
Reset output sink current (Note 4)	I_{OL1}	C	ON	OFF	B	ON	ON	ON	5.0 V	5.0 V	3.0 V	–	–	I_{O1}
	I_{OL2}	A	OFF	OFF	B	ON	ON	ON	5.0 V	5.0 V	3.0 V	–	–	I_{O2}
C_T charge current 1	I_{CT1}	B	OFF	OFF	B	OFF	OFF	ON	5.0 V	–	1.0 V	–	–	I_{CT}
C_T charge current 2	I_{CT2}	B	OFF	OFF	B	ON	OFF	ON	5.0 V	–	1.0 V	–	–	I_{CT}
Minimum power supply for $\overline{\text{RESET}}$ (Note 5)	V_{CCL1}	B	OFF	ON	B	ON	ON	ON	0 to 2.0 V	0 V	0 V	–	–	V_{O1}, V_{CC}
Minimum power supply for RESET (Note 6)	V_{CCL2}	B	ON	OFF	A	ON	ON	ON	0 to 2.0 V	0 V	0 V	–	–	V_{O2}, V_{CC}

NOTES:
1. Decrease V_{CC} from 5.0 V to 4.0 V and note the V_{CC} value when V_{O1} (observed on CRT_1) transitions to an abrupt LOW state.
2. Increase V_{CC} from 4.0 V to 5.0 V and note the V_{CC} value when V_{O1} (observed on CRT_1) transitions to an abrupt HIGH state.
3. Increase the Clock voltage (V_{CLK}) from 0 V to 3.0 V and observe the value of V_{CLK} when I_{CLK} transitions to an abrupt increase.
4. Measured with V_{O0} = 1.0 V.
5. Increase V_{CC} from 0 V to 2.0 V and note the V_{CC} value when V_{O1} (observed on CRT_1) transitions to an abrupt LOW state. The V_{O1} value will initially track the V_{CC} voltage increase until the internal circuit bias becomes active, at which time the V_{O1} value will return to a LOW state.
6. Increase V_{CC} from 0 V to 2.0 V and note the V_{CC} value when V_{O2} (observed on CRT_2) starts to track the V_{CC} voltage.

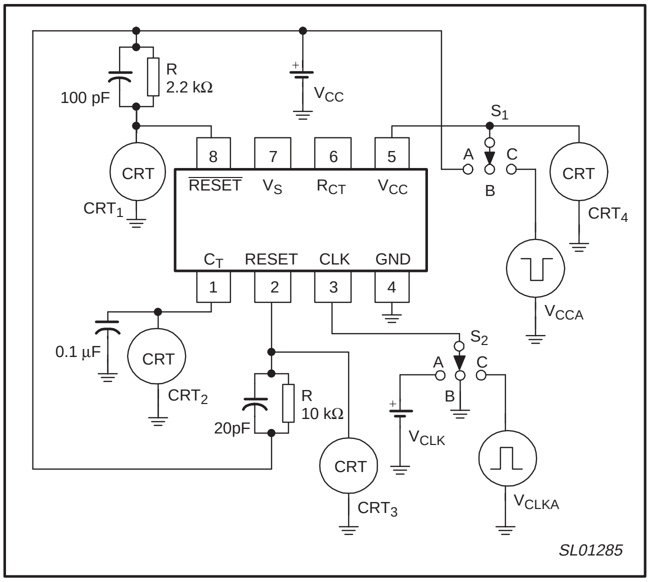
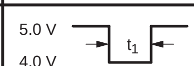
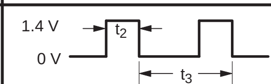
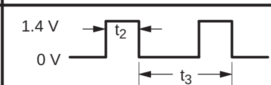
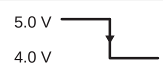
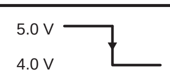


Figure 24. Test Circuit 2 (AC parameters).

Table 2. Switch and power supply settings, AC parameters

Parameter	Symbol	S_1	S_2	V_{CCA}	V_{CC}	V_{CLKA}	V_{CLK}	CRT
V_{CC} pulse width for detection (Note 1)	t_{P1}	C	C		–		–	1, 2, 3
Clock input pulse width (Note 2)	t_{CLKW}	A	C	–	5.0 V		–	1, 2, 3
Clock input cycle (Note 3)	t_{CLK}	A	C	–	5.0 V		–	1, 2, 3
Watchdog monitoring time	t_{WDM}	A	A	–	5.0 V	–	5.0 V	1, 2, 3
Watchdog reset time	t_{WDR}	A	A	–	5.0 V	–	5.0 V	1, 2, 3
Power-on reset delay time	t_{PR}	B to A	A	–	5.0 V	–	5.0 V	1, 2, 3
RESET, $\overline{\text{RESET}}$ propagation delay time	t_{PD1}	C	B		–	–	0 V	1, 2
	t_{PD2}	C	B		–	–	0 V	2, 3
RESET, $\overline{\text{RESET}}$ rise time	t_{R1}	A	A	–	5.0 V	–	5.0 V	1
	t_{R2}	A	A	–	5.0 V	–	5.0 V	3
RESET, $\overline{\text{RESET}}$ fall time	t_{F1}	A	A	–	5.0 V	–	5.0 V	1
	t_{F2}	A	A	–	5.0 V	–	5.0 V	3

NOTES:
1. t_1 = 8.0 µs.
2. t_2 = 3.0 µs.
3. t_3 = 20 µs.

PACKING METHOD

The NE56605-42 is packed in reels, as shown in Figure 25.

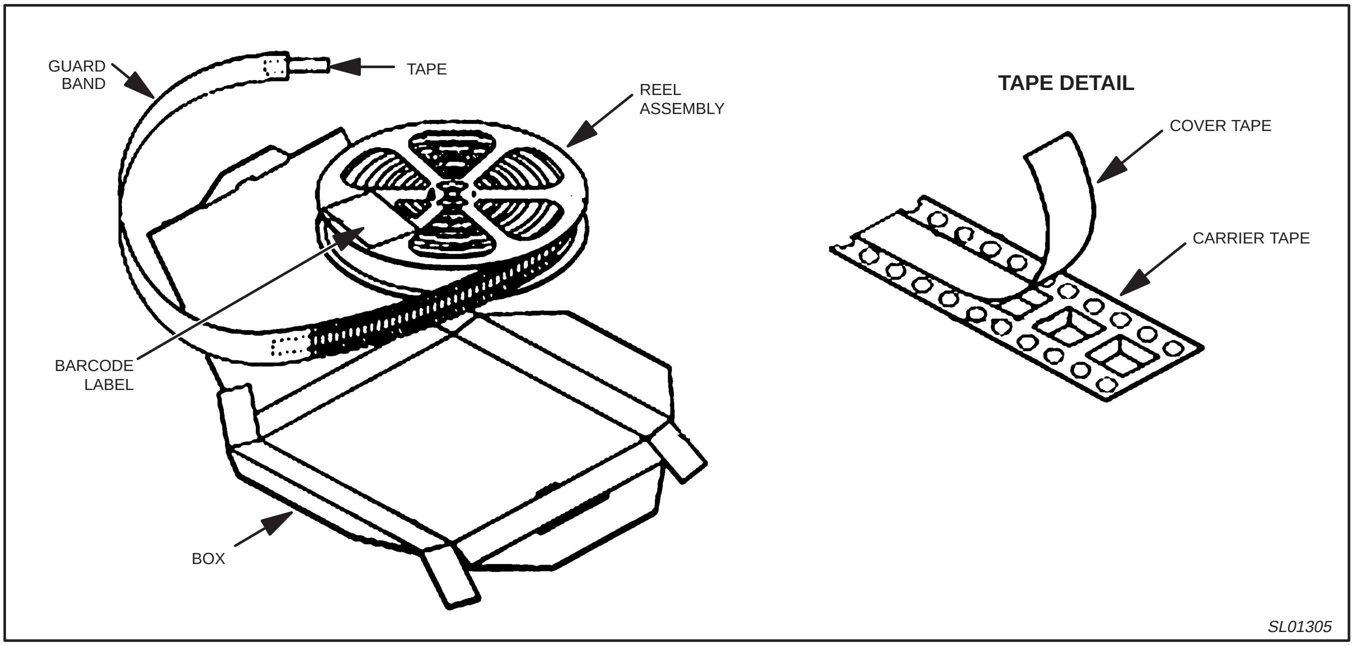
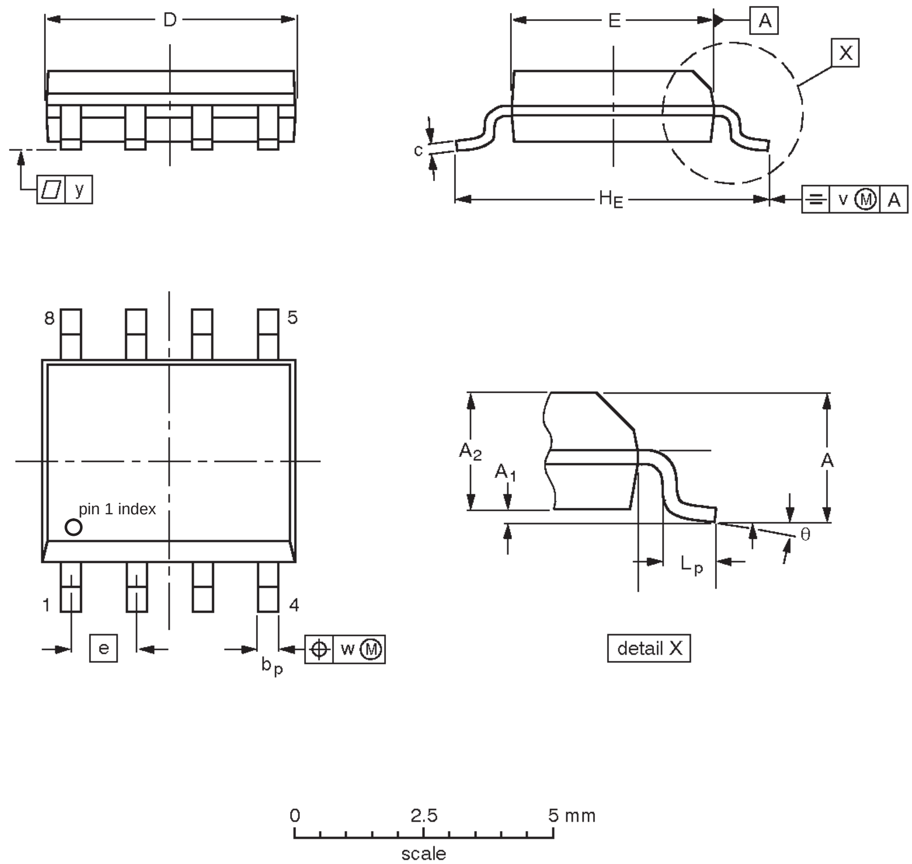


Figure 25. Tape and reel packing method

SO8: plastic small outline package; 8 leads; body width 3.9 mm



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	B_2	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E		L_p				y		θ
mm	1.73	0.25 0.10	1.45 1.25	4.95 4.80	0.51 0.33	0.25 0.19	4.95 4.80	4.0 3.8	1.27	6.2 5.8		1.27 0.38				0.076		8° 0°
inches	0.068	0.010 0.004	0.057 0.049	0.189 0.195	0.013 0.020	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228		0.050 0.015				0.003		

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			
	IEC	JEDEC	EIAJ	
SO8	076E03	MS-012		

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
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